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T H E S N S D A T A A C Q U I S I T I O N E L E C T R O N I C S

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1.0 INTRODUCTION

All neutron scattering instruments at the Spallation Neutron Source (Rutherford Appleton Laboratory) are connected to the PUNCH Data Acquisition and Display System. The PUNCH system encompasses all the hardware and software necessary to control instruments, acquire, manipulate, display and archive data. This paper describes the Data Acquisition Electronics (DAE) which is a subsystem of the PUNCH Data Acquisition System. The operation of the DAE within the overall system and functions of the individual modules of the DAE are described. The detailed circuit descriptions of the modules and the user guides for setting up and programming them are in preparation.

2.0 THE DATA ACQUISITION SYSTEM

Figure 1 shows a block diagram of the Data Acquisition System.

The scattering angles of the diffracted neutrons are defined by the detector positions. The outputs of these detectors are digitised, and in some cases encoded, by the detector electronics. This digital information is presented to the front end Instrument Crates of the Data Acquisition Electronics.

The input modules within the Instrument Crates generate a bit partitioned space - time descriptor for each detected neutron. The spatial information is provided by the detector electronics and the time information is a measure of the elapsed time since the SNS neutron pulse was produced, ie the time of flight of the neutron. Descriptors are stored on a frame by frame basis in the Instrument Crates (where a frame is a SNS cycle or number of cycles) before being transferred to the System Crate. This allows data for a frame to be rejected, if it is corrupted in some way, before being added to the total data acquired for the run.

Up to 20,000 neutron descriptors can be acquired in a frame, which when using 20mS frames corresponds to a 1MHz data rate. The Instrument Crates can acquire this data in a 10MHz burst. Peaks of up to 20MHz can be absorbed by FIFOS in the input modules.

The System Crate controls data acquisition and data transfer from the Instrument Crates via the Instrument Bus. The timing information used to generate the time partition of the neutron descriptors by the Instrument Crate is provided by the System Crate.

Descriptors transferred from the Instrument Crates have further information added to them relating to the elapsed time since the start of the run and are then processed to form the address of a large store. Data transfer then consists of incrementing the store location corresponding to each descriptor.

Facilities to monitor run parameters and implement test features are included in the System Crate. A computer interface allows the Data Acquisition Electronics to be controlled by the VAX 11/730 Front End Minicomputer and for data to be downloaded at the end of a run.

The Front End Minicomputers on each instrument are connected to a Cambridge Ring Local Area Network, as is a central hub computer and gateways to the laboratory central computers and SERC network.

3.0 THE DATA ACQUISITION ELECTRONICS (DAE)

In order to accommodate the needs of different instruments a modular system has been developed.

Figure 2 shows a block diagram of the DAE. Most of the modules use wire-wrap construction and have been designed using the laboratory's CAD facility. The Instrument Crate input modules use multi-layer printed circuits.

3.1 INSTRUMENT CRATE

The Instrument Crate uses CAMAC standard mechanical components together with a custom design printed circuit backplane, the Instrument Crate Bus. Power supplies are mounted on the back of the crate. A system can contain up to 16 Instrument Crates, each crate containing an Instrument Crate Controller, a pair of Ping-Pong Frame Memories and up to 16 Data Input Modules.

3.2 DETECTOR INPUT MODULES (DIM)

There are 3 types of DIM modules:

DIM1 A module with 8 parallel inputs, each with its own FIFO. The output descriptors contain the time information and a 3-bit position code for the corresponding event.

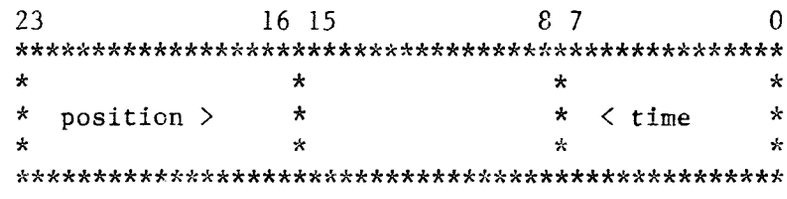
DIM2 A module with a 12-bit binary coded input and a single FIFO handling 4096 channels. The output descriptors contain the time and position code for the corresponding event.

MIM A Monitor Input Module with 4 parallel inputs designed for neutron beam monitoring. Each input has an 8-bit binary prescaler, presettable by switches in the module. The output descriptors contain the time information corresponding to the last event in a prescaled group, and an associated 2-bit position code.

If a FIFO in any of the DIM modules overflows during data taking a flag is set in the Instrument Crate Controller.

3.3 INSTRUMENT CRATE BUS

The bus uses ECL technology and can read data from the DIMs at up to 10 MHz. Modules will issue requests to the Instrument Crate Controller when they have data to transfer. They will be serviced on a fixed priority basis. The bus is 24 bits wide and partitioned as shown in the diagram:



The position of the partition can be varied over the centre 8 bits on a crate by crate basis. The timing parameters for the instrument must be set to prevent overflow into the position partition and the Descriptor Generator in the System Crate must be set up appropriately. There is also a 16 bit time channel bus driven by the Instrument Crate Controller to provide Gray coded time information to the DIMs.

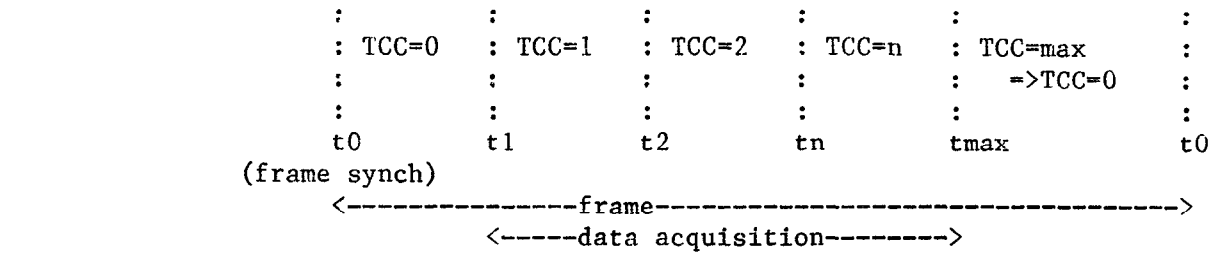
3.4 INSTRUMENT CRATE CONTROLLER (ICC)

The ICC controls data acquisition in the crate and provides the interface to the Instrument Bus.

The synchronous data acquisition controller carries out the priority arbitration on the DIM request signals, and generates the necessary timing signals to read the descriptors from the DIMS and load them into the Ping-Pong Frame Memories.

The module contains the Gray coded time channel counter which is incremented by the external time channel increment signal. The time channel counter is reset by the frame synch (t0) or when a preset maximum time channel count is reached. This maximum value is set in the ICC by the host computer via the Instrument Bus. Data acquisition is inhibited when the time channel counter = 0.

Timing definitions are illustrated below:



TCC=Time Channel Count

3.5 PING PONG FRAME MEMORY (PPFM)

The PPFM is linked to the ICC by a front panel Instrument Crate Controller Bus. The Instrument Crate contains two modules each containing 20k*28 bit (24 bits + 4 bits module address) of RAM for one frame of data. Data acquisition and data transfer alternates between the two modules on a frame by frame basis. Data acquisition refers to the real time acquisition of data using the Instrument Crate Bus where the descriptors are stored sequentially in a PPFM. Data transfer refers to the downloading of a PPFM to the system Crate and subsequent operations including the Read-Increment-Write operation on the Bulk Store.

Registers within the PPFM's contain the word count, and flags to indicate if the PPFM overflowed or if a FIFO overflowed in the corresponding data acquisition cycle. These registers are normally read by the Instrument Bus Interface via the Instrument Bus and ICC prior to data transfer.

3.6 INSTRUMENT BUS

The Instrument Bus is a daisy chain bus linking the ICCs to the Instrument Bus Interface (the bus controller). It is used to set up the maximum time channel count in the ICCs, read the ICC status registers, and download data during data transfer operations. Data can also be written to the PPFMs for the test purposes.

The bus uses twisted pair cable carrying ECL balanced signals with a maximum length of 30m. Data transfer can take place at up to 1MHz.

3.7 SYSTEM CRATE

The System Crate uses Intel Multibus standard cards and signal definitions. The crate is a custom design and incorporates power supplies.

10 card slots are provided at a 1" pitch for wire wrap cards, 8 slots are provided at the standard 0.6" pitch for printed circuit cards, this section being intended primarily for the Bulk Store memory cards.

Only serial priority arbitration is supported since there are only two bus masters, the Computer Interface and the Incrementer.

Up to 16 System Crates, and therefore 16 sets of Data Acquisition Electronics, can be attached to each Front End Minicomputer.

3.8 INSTRUMENT BUS INTERFACE (IBI)

The IBI controls Multibus access to the Instrument Crates via the Instrument Bus. The Instrument Crate registers are mapped directly into Multibus I/O address space.

The IBI also controls data acquisition and transfer.

A bit in the IBI control register determines whether or not the system is acquiring data. Data acquisition is not allowed for part frames and the IBI carries out the necessary synchronisation to avoid this. When the data acquisition bit is negated the IBI will generate an interrupt (which can be disabled via the control register) and reset a data acquisition status bit when data acquisition has finished and the last acquired frame of data has been transferred to the Bulk Store.

At the start of each data transfer frame the IBI reads the status register in each ICC and determines the total number of descriptors acquired in the previous frame, and whether any of the PPFMs or FIFOs overflowed. Under certain conditions the frame will be vetoed, ie. the data will not be transferred and will be lost. The conditions are:

(1) An external veto was received during the frame.

(2) The total descriptor count exceeded 20,000.

(3) A PPFM overflow was flagged.

(4) A FIFO overflow was flagged.

(5) A proton count underflow was flagged.

(6) A chopper out of phase veto was received.

Each of the 6 conditions can be enabled or disabled by bits in the IBI control register. The system is designed to eliminate, as far as possible, the loss of part of a frame of data. If data transfer from a particular frame is still taking place when a frame synch is received the data transfer will continue until complete. Meanwhile data acquisition will be halted. The halting and restarting of data acquisition will only take place on frame boundaries.

If a frame's data is lost due to overrun of data from the previous frame or if there was an enabled veto condition present the IBI will generate an interrupt (this can be disabled via the control register). A status register will contain the reason for the interrupt.

The IBI transfers data from the PPFM in each Instrument Crate to the Incrementer via the Neutron Proton Monitor and Descriptor Generator. The IBI adds the crate address (4 bits) and the frame count (8 bits) to the incoming descriptors, making a total descriptor of 40 bits.

There is a frame count prescaler (up to /256) presettable from the Multibus. The value of this prescaled frame count, which forms the frame count position of the descriptor, can be read from the Multibus.

There are also registers containing the frame count during the run and the number of frames of data transferred.

3.9 DESCRIPTOR GENERATOR (DG)

The 40-bit descriptor passed to the DG by the IBI is compacted to form an address within the range of the Bulk Store. The following functions are performed and are programmable from the Multibus.

(1) bit partitioning of the 24 bit time/position component of the descriptor from the DIMs, using a look-up table addressed by the crate address to control a multiplexer.

(2) concatenation of the position descriptors, by adding constants from a look-up table addressed by the module and crate addresses. Up to 16 bits are allowed for the concatenated position descriptor.

(3) a 64k*16 bit look-up memory addressed by the concatenated position descriptor, allows any ganging or bit routing patterns to be set up for the position descriptor.

(4) position and time descriptors are merged using a t+(tmax*p) algorithm.

(5) position time descriptors are concatenated and the frame number included by adding a constant from a look-up table addressed by the frame count and crate address.

The compacted descriptor is passed to the Incrementer.

3.10 INCREMENTER (INR)

During data transfer the INR controls the Multibus and performs Read-Increment-Write operations on the Bulk Store locations corresponding to the incoming descriptors. The INR supports 8, 16 or 32 bit word length in the Bulk Store. If a Bulk Store location overflows the location is set to zero, the address stored in a 32 word FIFO accessible from the Multibus and an interrupt is generated.

3.11 NEUTRON PROTON MONITOR (NPM)

The Frame Synch pulse provides the basic time reference for data acquisition and transfer and for neutron time of flight measurement. The NPM normally derives this signal from an external source but an internal oscillator and Multibus controlled single shot facility are available for test purposes. The external source can either be the SNS control system,

or the chopper control system in cases where a chopper is being used to delete pulses of neutrons. The Frame Synch can be delayed with respect to the source by up to 256mS with 4μS resolution (programmable from the Multibus).

In addition the NPM accumulates externally generated neutron and proton counts and the neutron count from predetermined DIMs or MIMs.

A ten bit proton count for each frame is passed to the NPM which compares the count with a presettable value. If it is below this a proton count underflow veto is passed to the IBI. The total proton count for the run is accumulated as a raw proton count, the counts associated with frames of data transferred are accumulated as a good proton count.

The neutron count for the frame is passed to the NPM as a series of pulses which are counted after passing through a programmable time gate. As with the proton count raw and good neutron counts are accumulated for the run.

The NPM monitors the descriptor transfers between the IBI and DG. Descriptor and mask registers allow two separate selected descriptor counts to be accumulated. The 16 bits of the descriptor position partition and the crate and module address partitions are monitored. The mask register allows 'don't care' bit positions to be programmed into the descriptor selection.

For test purposes the NPM can drive the DG input directly, the IBI output drivers can be turned off for this purpose.

3.12 TIME CHANNEL GENERATOR (TCG)

The TCG uses a RAM look up table to generate the time channel increment pulses to be routed to the ICCs.

A 20 bit scaler is clocked by a 32MHz crystal clock giving 32nS resolution and 32mS full scale. A 32k*20 bit RAM is loaded with the required time channel boundaries from the Multibus. These are fetched in sequence, the

increment pulses being generated by comparison with the scaler output. The minimum time channel width is determined by the memory access time and is 500nS. There is a 3 bit binary clock prescaler, programmable from the Multibus, to accommodate frames longer than 32mS. Using the prescaler frames of up to 8x32mS may be accommodated. The time channel increment pulses are transmitted on 16 separate ECL twisted pair lines to the ICCs.

Instruments can have more than on time regime (but not crossing crate boundaries) by adding more TCGs.

3.13 BULK STORE

The Bulk Store is implemented using commercial memory modules. In current technology these are available in sizes of up to 4 Mbytes. The Multibus can support up to 16 Mbytes of memory.

The memory cards have error detection circuits which will generate an interrupt if a parity error occurs. These interrupts can be disabled.

3.14 COMPUTER INTERFACE (CI)

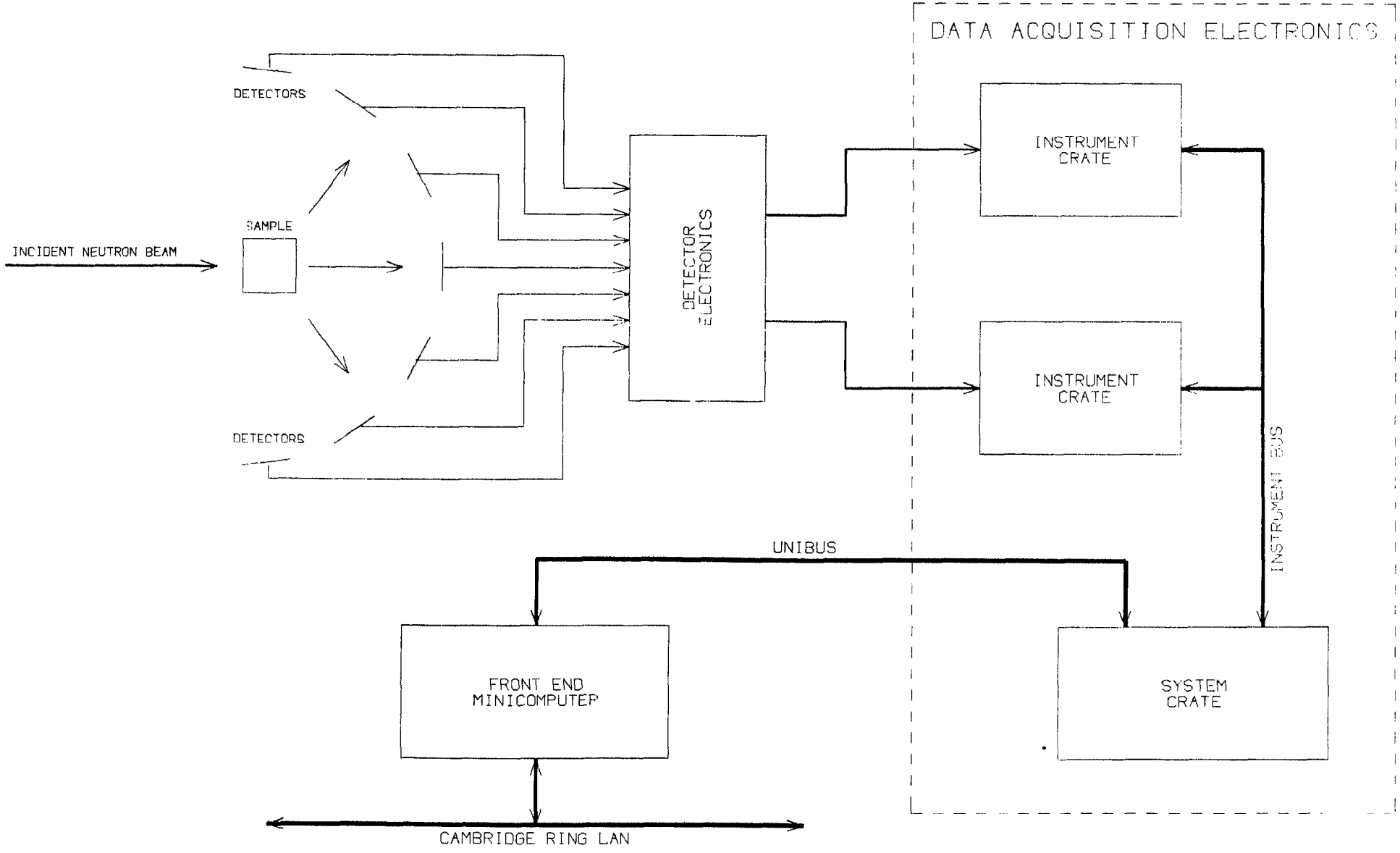
The CI interfaces the DEC Unibus from the VAX 11/730 Front End Minicomputer (FEM) to the Multibus.

The Bulk Store appears directly in the memory address space of the Multibus using all of the 16 Mbyte address range if required. The Unibus accesses Multibus memory address space via an auto-incrementing address register and a memory data register in Unibus user I/O address space. Other System Crate module registers will be in Multibus I/O address space accessed using the same address register (but not auto incrementing for I/O accesses) and an I/O data register. These module registers include auto-incrementing address registers and associated data registers to access look up table memories.

Bidirectional DMA transfers are supported between the FEM and Multibus memory and I/O address space. Block, burst and single shot DMA modes are provided.

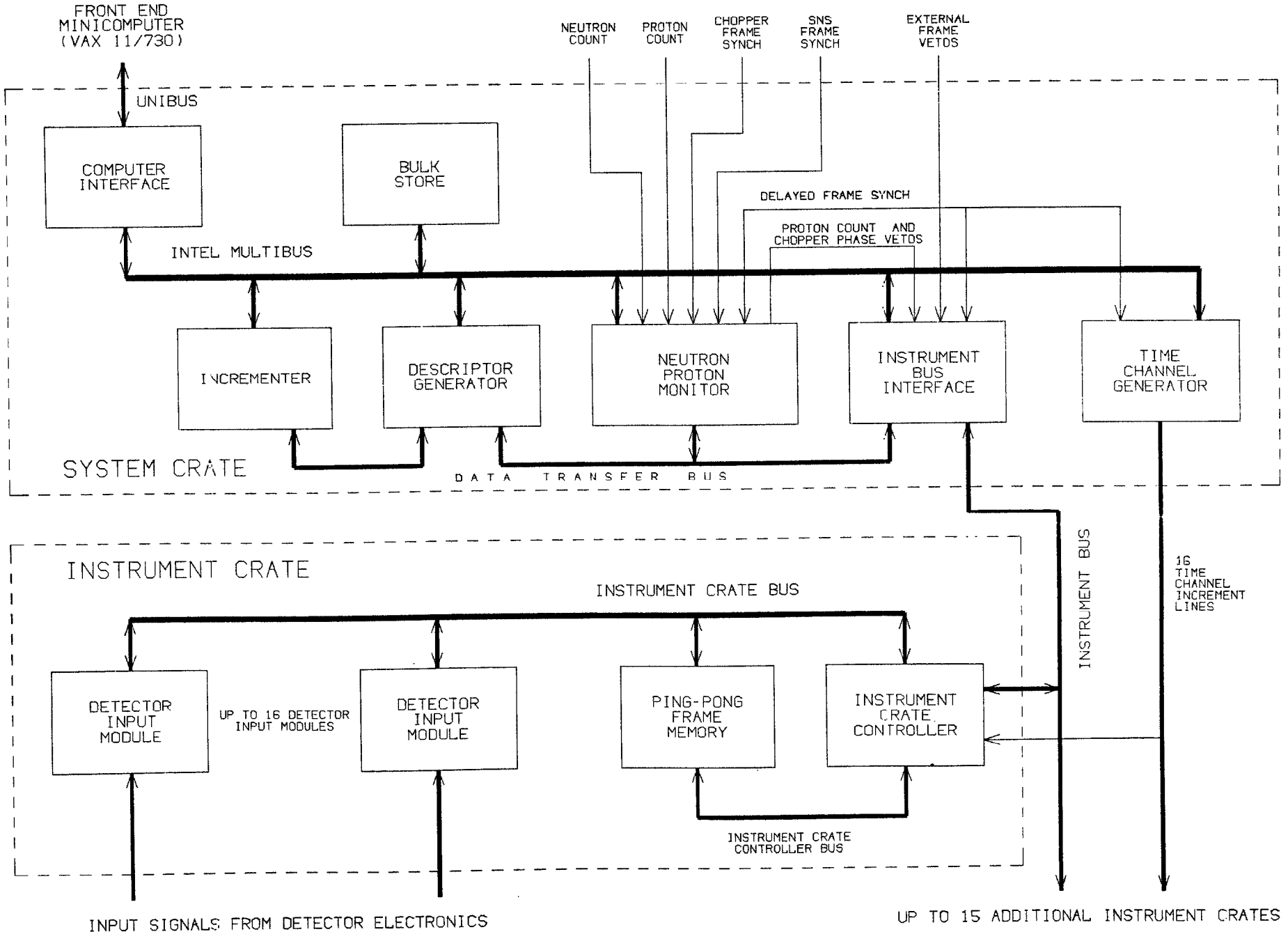
An interrupt can be generated to the FEM through a hardware presettable vector and at a hardware presettable priority level in response either to a Multibus interrupt or the end of a DMA operation.

The interrupt sources can be individually disabled. In the case of a Multibus sourced interrupt a register in the CI contains the bit pattern of the Multibus interrupt level(s) that crused the FEM interrupt.



SNS DATA ACQUISITION SYSTEM

FIGURE 1



SNS DATA ACQUISITION ELECTRONICS

FIGURE 2