

THE ISIS SECOND GENERATION DATA ACQUISITION ELECTRONICS

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Abstract

The ISIS Data Acquisition Electronics has been in successful operation since 1984. However, improving neutron detector technology, an ever-changing computing environment and more exacting experiments are challenging its design specification. A second generation data acquisition electronics system is needed to accommodate increased detector numbers and allow more varied data acquisition control and monitoring. Real-time display and a pre-processing capability of the acquired data are also required. This paper outlines the current electronics, the issues that dictate the need for change and the new system that will replace it.

I. INTRODUCTION

The design of the existing ISIS Data Acquisition Electronics was first proposed back in 1979. Its specification was derived from detailed discussions between the instrument scientists and the Rutherford Appleton Laboratory's Electronics Division. Three systems were commissioned for the first ISIS neutron run in December 1984. Since then, the number of systems has grown to fourteen, with two 'hot spares' used for testing and evaluation purposes. Although each ISIS neutron scattering instrument differs in characteristic, it is the same data acquisition electronics design that supports them all.

II. THE ISIS DATA ACQUISITION ELECTRONICS

A. System Overview

The Data Acquisition Electronics (DAE-I) is an integral part of the ISIS PUNCH Data Acquisition and Display System. It is made up of two component parts, the Instrument and the System Crate (See Fig. 1). The Instrument Crate is connected to the detectors via detector processing electronics. Its role is to capture the detected neutron position with a corresponding time-of-flight timestamp to form a descriptor word. The System Crate is responsible for generating the acquisition timing, processing the descriptors, and histogramming them. This crate is attached to the Front End Minicomputer (FEM) which controls the whole acquisition process.

As many as 16 Instrument Crates can be attached to a single System Crate. Generally, the Instrument Crates reside close to the detectors whilst the System Crate is located near the FEM in the instrument cabin. A maximum distance of

30Metres between the two crate types can be catered. This is achieved by a three cable interconnection of a 28Bit good descriptor data bus, an acquisition timing signal bus and an acquisition control signal bus. All these interconnections use balanced complimentary ECL signals in twisted pair format to cope with the long distance between crates and to counter externally generated noise pickup. In a multiple Instrument Crate implementation this interconnection is daisy chained between the crates.

The Instrument Crate is based mechanically on CAMAC but with an in-house designed backplane incorporating a detector readout bus. This bus can achieve a peak raw descriptor readout rate of 10MHz from the detector modules. The raw descriptor is partitioned into a 24Bit wide detector position and time-of-flight descriptor word part. The backplane also contains the 16Bit time channel bus which distributes the time-of-flight descriptors to the detector modules. The System Crate uses the standard Multibus-I bus architecture with its 24Bit address and 16Bit data bus. The read and write operations are undertaken as a command from a master card and completed by an acknowledge issued from an accepting slave card. The bus is used in three ways, to set up parameters within the System Crate cards defining the experimental run, to perform the histogramming process and finally to readout the histogram data.

B. The Instrument Crate

The Instrument Crate modules and their functionality will now be described. There are two types of input module in which data is captured. These are Instrument Beam Monitor Modules (MIM's) and Detector Input Modules (DIM's) of which several variations exist. The DIM1 module takes data from 8 independent detector inputs, whilst the DIM2 module accommodates 4096 detectors through a 12Bit binary coded input. Lastly the DIM3 module encodes upto 64 detector inputs into a 6Bit coded event position word. The MIM module accepts 4 beam monitor inputs. Apart from the input stages, both MIM's and DIM's follow the same design. An input latch captures the neutron position and the time-of-flight word. This is stored in a 16Word deep Last-In-First-Out (LIFO) memory. A peak event input rate of 20MHz can be absorbed by each module. If event data is written into the LIFO quicker than it can be readout, then the module can flag a LIFO overflow veto.

The 24Bit raw descriptors output from the monitor/detector modules are stored in two Ping-Pong Frame Memory (PPFM) modules, on an acquisition frame by frame

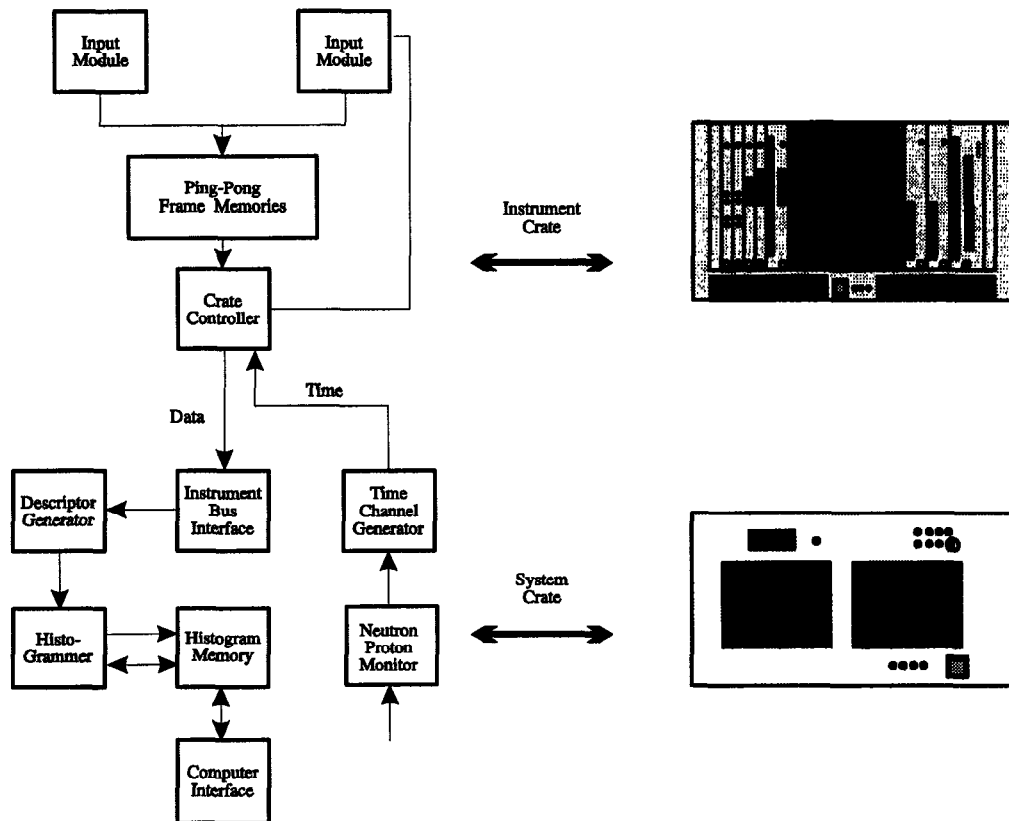


Fig. 1. The DAE-I Electronics

basis. Whilst one PPFM is acquiring descriptors the other is transferring descriptors to the System Crate. Each module contains 20KWords of SRAM, where each word is made up from the 24Bit raw descriptor and a 4Bit MIM/DIM identifying word. The number of descriptors acquired in a frame is counted and if this goes above 20000, then a PPFM overflow is flagged. This veto and a crate global MIM/DIM LIFO overflow are checked prior to data transfer to be ensure that the collected data is valid.

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The last module in the Instrument Crate is the Instrument Crate Controller (ICC). It determines the arbitration of input modules seeking permission to write raw descriptors into the PPFM. The modules are serviced on a priority basis, with the priority determined by the module position. A second function it has is to generate the 16Bit time-of-flight channel bus words which are required by the

input modules. Its final role is to handle the transfer of the PPFM descriptors to the System Crate, generating the required bus timing protocols.

C. The System Crate

The System Crate splits into seven functional component parts. The Neutron-Proton Monitor (NPM) covers three cards. One of these is responsible for the timing and synchronisation of the data collection to the ISIS neutron pulses. It takes in the ISIS Frame Synch pulse (or a chopper system synchronising pulse), and adds a user-settable delay before distributing it as the Delayed Frame Synch time reference, for the Instrument Crate data acquisition and transfer. Run data logging is also performed within this group of boards. This data includes the good/raw accumulated beam current values received from the Protons-Per-Pulse (PPP) Receiver card.

The Time Channel Generator (TCG) card is responsible for setting up the time channel boundaries in the histogrammed spectra. On this card is a 32KWord lookup table holding the time channel boundaries relative to the Delayed Frame Synch pulse. A 32MHz clock drives a counter which generates a word for comparison with the first time channel boundary word in the lookup table. When they are equal a pulse is sent to the ICC which increments the 16Bit time-of-flight word to the input modules. This continues until either the maximum number of time channels is reached or the

next ISIS pulse occurs. These conditions reset the lookup table back to its beginning.

The Instrument Bus Interface (IBI) control and driver cards initiate the data collection process and readout the PPFM 28Bit descriptors synchronised to the Delayed Frame Synch pulse, at a rate of 1MHz. It adds the Instrument Crate address (4Bits), and Period Count (8Bits), generating a 40Bit descriptor which is then pipelined through the other cards in the System Crate. The second function of the IBI is veto handling, where something external has gone wrong in an acquisition frame, with likely data corruption resulting. The IBI would flag to the Instrument Crate not to transfer that particular frame. Included in this veto monitoring are the detector/monitor input module global LIFO and PPFM overflow veto's sourced from the Instrument Crate. Also external vetoes such as chopper out of phase and moderator temperature are monitored. The IBI also holds counts of the number of raw and good (transferred) PPFM data frames.

The 40Bit descriptor passes to the Descriptor Generator, (DG) which is responsible for mapping it to a 24Bit histogram address. Various on-board lookup tables allow efficient mapping which includes the ability to gang detectors to a particular spectra. The 24Bit output of the DG is passed to the Incrementer card (INC) which performs the actual histogramming process by generating Read-Increment-Write cycles to the Histogram Memory (HMEM). As much as 16MBytes is available to be used as Histogram Memory.

The final stage is the Computer Interface (CI) linking the System Crate to the FEM via DEC's QBus standard. The card contains QBus mapped registers controlled by a software driver resident on the FEM. These registers act as gateways to the System Crate histogram and run set-up address locations. Within the System Crate this card acts as master sharing this role with the Incrementer. Arbitration logic between the two cards allows dual access to the Histogram memory.

D. DAE-I Software Interaction

A brief overview of the DAE-I software interaction is necessary to highlight some of the problems now being faced by DAE-I.

The most important interaction occurs through the Instrument Control Program (ICP). This allows the user to set-up detector to spectra mappings, time channel widths and veto enables. When these parameters are ready then a BEGIN can be typed at the terminal screen. This has the effect of clearing the histogram memory, setting up the various lookup tables and initialising registers and counters. The final operation is to set a control bit within the IBI which instructs data acquisition to start on the next ISIS Frame Synch pulse. Each of these memory/register access operations is undertaken by the FEM, which means that for large histogram instruments there is a delay of ten's of seconds before the run starts. This is also apparent when an END instruction is typed, where the

histogram memory contents are readout with the total number of frames and the total accumulated beam current.

Another DAE-I software interaction is with the DASHBOARD process. Approximately every five seconds the good/raw frame counts, the beam current, and monitor counts between pre-set time limits are readout. In the case of the monitor counts, a block access to the histogram is made and the integrated counts calculated in the FEM. The problem here is with the randomness to which this process access's the DAE, holding up the transfer of data from the PPFM to the histogram memory. Also the block transfer of the monitor counts data is inefficient.

The other major interaction with the DAE-I can be done through the GENIE spectra display and manipulation software. It has a command which allows runtime access to the DAE-I histogram memory so that whilst the run is executing, the detector spectra can be displayed. Again the randomness of this access and the ability to examine multi-spectra plots (large block data transfers) tends to hold up DAE-I descriptor transfer and histogramming.

III. THE NEED FOR CHANGE

The forward looking design of the DAE-I system has enabled it to cope with many instrument design changes. After some nine years of continuous operation, it is only now that the design of ISIS Instruments are starting to stretch its operation. This section looks at those factors influencing the need for change.

A. Expanding Data Acquisition Parameters

With the increase of detector numbers through continual instrument upgrading, the most pressing issue on DAE-I is the histogram memory size. This is related to the number of detectors the instrument has, and the number of time channels used to 'time stamp' the detected event. The amount of memory store allocated to hold the number of counts for each event histogram channel is also important. This must be large enough to avoid data loss through count overflows. This store can be programmed to 8, 16 or 32Bits long but is generally set to the latter. The current DAE-I histogram memory is thus limited to 4MEvent histogram channels, restricted by the 24Bit (16MBytes) addressing range of the System Crate Multibus-I backplane.

The 16MByte histogram limit is now being reached by ISIS Instruments SXD and MARI. The detector upgrades for SANDALS, SXD and the SURF detector system easily surpass this limit as shown in Table 1.

Another issue concerns long flight path instruments such as HRPD and IRIS. Within DAE-I both the incident beam monitor and detector time-of-flight data share the same time regime. Where the monitor is close to the detector this is fine, but where there is some distance between the two, the resulting monitor spectra needs some manipulation before

normalisation can take place. Hence the need to run the monitors and detectors on different timing regimes relative to the ISIS Frame Synch Pulse.

Instrument	Detector Elements	Time Channels	Histogram Memory
SANDALS (1994)	1500	5000	30MBytes
SXD (1994)	2 x 4096	4000	128MBytes
SURF (1995)	20000	2000	160MBytes

Table 1. Instrument Future Histogram Requirements

A final point concerns the introduction of glass scintillator detectors to EVS. This has increased the overall detector event rate for the instrument. Whilst the DIM peak input rate of 20MHz is not reached, the overall event rate readout to the PPFM's shared across four DIM modules is approaching the DAE-I limit of 10MHz.. There is also the implication that more than 20KEvents could be collected per frame, thus overflowing the PPFM's. The ability to scale data acquisition to accommodate higher event rate detectors in a manageable way is necessary.

B. Instrument Diagnostics

This area concerns the ability of the DAE to be used as an instrument fault diagnostic tool. A major concern is DAE-I's lack of effective handling of a detector going noisy. The Instrument HET used to minimise the number of detector spectra by ganging detectors together in the Descriptor Generator lookup tables. However a detector going noisy within a group corrupted the ganged spectra and the instrument reverted back to individual detector spectra. The second problem concerns identification of that noisy detector. In the DAE-I Instrument Crate each monitor/detector module LIFO output is ganged together to produce a single LIFO overflow veto. Because of the ganging it makes identification of a noisy detector, within a module, and/or within a crate of modules difficult to trace. It is therefore necessary to be able to trap and identify this faulty condition quickly.

Another problem relates to the moderators and their performance in the ISIS target station. Current moderator performance is monitored by software taking neutron and proton counts periodically and displaying the results over a 24Hr time frame. This method tends to reveal problems only after trouble has occurred with potential data corruption in the spectra. The ability to compare the proton value with the incident beam monitor counts on a frame by frame basis and veto the acquired frame if outside a tolerance, would minimise data corruption and flag to the user quickly that something is wrong.

A further related veto issue is the ability to identify which veto condition is causing problems. With DAE-I, the

only way that vetoes are noticed is when there is a mismatch between good and raw frame counts. This doesn't reveal the source nor identify trends where for example a chopper phase veto may increase its occurrence over many runs signifying a degradation in chopper performance.

C. Data Pre-Processing

Increasing the histogram memory size to accommodate extra detectors has further consequences for the DAE. The time taken to transmit the histogram between the DAE-I histogram memory and the FEM is important. If these transfers become too long they could delay the start of the next data acquisition run. The transfer rate between the DAE-I and FEM is 100KBytes/sec and is limited by QBus and the controlling software.

Another consequence of larger histograms is the time it takes for the FEM to clear the histogram ready for the next run. This is already approaching nearly a minute to clear 8MBytes of memory. It is currently undertaken by the FEM issuing block writes of zero data into the histogram memory locations. This is an unnecessary drain on the FEM computing resource. Also the block reading of the monitor counts between time limits seems an inefficient use of the interconnecting bus.

Methods of efficiently using the DAE/FEM interconnecting bus in control and data transfer need to be considered. One way is to introduce some pre-processing of the data. Rather than sending single bytes of DASHBOARD information, a packet of runtime data could be assembled and a block move of that data transferred. Further pre-processing would come in the form of data compression techniques used to minimise the size of the large histograms before data transfer.

IV. THE NEXT GENERATION DAE

A. System Overview

Like the current DAE-I, the second generation data acquisition electronics (DAE-II) is based on two crate types, the Interface Crate and the Control Crate (See Fig. 2). The Interface Crate is the link between the detector processing electronics and the Control Crate. The many different detectors offering varying types of connectors, electrical level and transmission formats, has led to many interface cards being built. Therefore, there is a need to buffer the more expensive control crate cards from these varying interfaces. The interface modules will cater for the standard DIM1 and DIM2 detector outputs, routing the signals into a high density 68-way shielded connector. Crate fan and power supply failure monitoring will be done on selected modules. Notification of a faulty condition will be sent to the Control Crate as a veto signal.

The Interface Crate can be either a CAMAC Crate or a DAE-I Instrument Crate. Interface modules running in these

crates will only be drawing power from the backplane, so no adaptation of these crates is required. The reason for choosing these crates is that they are well designed, known technology with ample power supplies and spares available. In re-cycling the DAE-I Instrument Crate this also circumvents a disposal problem as more DAE-I systems move to the DAE-II solution.

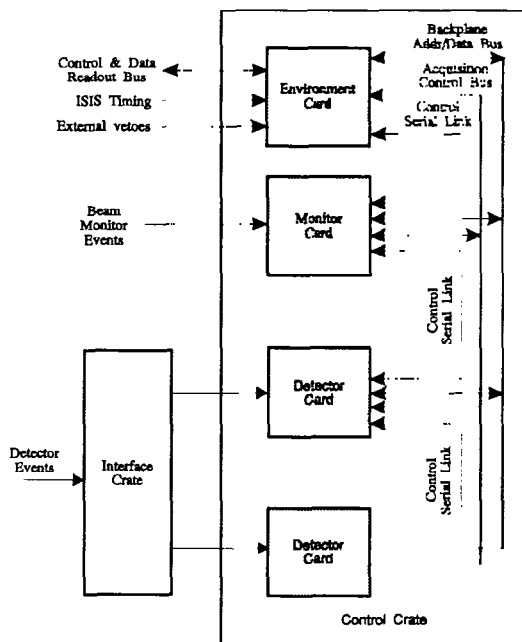


Fig. 2. DAE-II System Block Diagram

The DAE-II Control Crate is based on the VME Extended for Instrumentation (VXI) Bus [1]. The reason for choosing VXI is that it conforms to the VMEBus standard, which is well understood and proven technology. But VXI extends VME by introducing an inter-card daisy chain bus, dedicated inter-slot lines, more bus lines and extra power supplies. The enclosure provides an almost continuous surround of metal to minimise electromagnetic interference. Attention to this issue is becoming more and more important because of the increasing background electrical noise within the ISIS experimental hall.

All cards and modules will be manufactured in multi-layer PCB technology as oppose to the DAE-I which was fabricated using wirewrap. A PCB implementation will improve reliability with inner layer ground planes aiding screening as well as minimising ground bounce induced false triggering. For the Control Crate cards, a VXI D size card will be used. This 9U board size allows a high density of components to be laid out with fewer inter-connections needed. Further screening will be achieved by adding card sidecovers that will connect to the ground plane and totally enclose the card.

Surface mount components will help in making effective use of the board real estate. Also much use will be made of Programmable Logic Devices (PLD) and Xilinx Field Programmable Gate Arrays (FPGA) [2]. These allow many

standard logic gates to be programmed into a single package so reducing interconnections and increasing reliability. The reduced component inventory and re-programmability make these devices very attractive.

Three cards will exist in the Control Crate. These are the Environment card, the Monitor card and the Detector card and will now be described.

B. Environment Card

The function of Environment Card is two-fold, to act as the interface between the FEM and DAE, and to generate system data acquisition timing/control signals. A major change to the DAE environment is the FEM moving away from the MicroVax 3200 QBus series machines to the more powerful Alpha and SCSI workstations. For this reason the FEM/DAE-II interconnect bus chosen is SCSI-2 [3]. This is a proper communications bus geared towards block data transfers with error checking built-in.

The DAE-II SCSI interface will run either in 10MBytes (8Bit) SCSI-1 mode or at the full SCSI-2 mode at 20MBytes (16Bit). Which mode is used depends on the SCSI implementation in the workstation. Currently the DEC workstations support 8Bit mode. Single-ended and differential transmission formats will also both be supported allowing flexible positioning of the crate. Both Target and Initiator modes will be allowed enabling the DAE to act as a receiving data slave and/or as a bus master sending data to the workstation.

To set-up the SCSI interface, control data acquisition and readout/pre-process the histogram data an on-board processing element is required and this will be a Transputer [4]. This is a powerful microprocessor, simple to interface and has the ability to easily undertake parallel tasks with other Transputers. The Transputer board controller will be a 20MHz T805 floating point processor. It will have access to 16MBytes of DRAM for program workspace, 4MBytes EPROM for the program itself and 0.5MBytes Flash EPROM for runtime program variables. This last type of storage memory will be used to store parameters about the DAE configuration (how many cards, how much memory, etc.) and current run parameters (such as what vetoes are enabled, and time channel boundary information). This is necessary in case the Transputer descends into an error condition and needs re-initialising. The design of the data acquisition parts of the system will ensure that data acquisition continues in the event of this happening.

The VME Interface will be undertaken by an commercial VME Interface ASIC handling all the bus single cycle/block accesses, interrupts, master/slave bus arbitration and DMA control. Like the SCSI Controller it is set up and controlled by the Transputer. Bus transfer rates can be up to a maximum of 40MBytes/sec using 256Byte block transfers. The interface will be able to function as a master device, issuing read/write commands to other devices, or as a slave

receiving read/write commands. It will support 32Bit aligned and unaligned transfers over a 4GByte addressing range.

The VXI additions to the VME standard bring extra bus and interslot lines to the backplane. The bus lines will be used to distribute the ISIS Frame Synch pulse, a System DAQ Running flag and other DAQ control signals so as to synchronise all the cards in the system. The inter-slot lines will be used to distribute the Transputer 20MBit/sec serial links. It is envisaged that these links will be used to transfer small packets of data, leaving the larger histogram, block transfers to be done over the VME.

Turning to the system data acquisition control, this will be performed by several FPGA's. The Card FPGA has the responsibility for resetting the system and synchronising the run to the ISIS Frame Synch pulses. It will also distribute these signals to other cards in the crate.

The chopper FPGA will look after all the control logic concerned with running the DAE from a Chopper system. This includes generation of the DAQ Frame Synch pulse and the monitoring of the chopper out of sync with the ISIS neutron pulse. This will generate a veto which will be logged by a veto counter. Also in this FPGA will be a user-settable window that will monitor a Fast Fermi Chopper position pulse. If the position pulse falls outside the window then a veto is generated, and again this will be logged.

The new neutron-proton ratio veto will be on this card. A small lookup table will be loaded with values corresponding to the particular target. When the delivered proton value arrives, this is latched into the lookup table which generates a high and low band value to compare against the accumulated Incident Beam Monitor neutrons count. Towards the end of the frame the test is made to see if the actual neutron value lies within the band. If it does not then a veto is raised.

Another new feature on this card is what is labelled the Diagnostic Pulse Generator. This is essentially a replication of the TCG sub-circuit where values are loaded into a lookup table and compared with a running counter value. A trigger signal can be generated when the counter and lookup table values match. This is useful when trying to relate a noise spike appearing in the spectra to a detector signal allowing an oscilloscope to trigger precisely around the noise spike's position in time. The detector's signal at that point can then be inspected for strange pickup effects.

The Transputer/VME/VXI sub-system parts will be replicated on the Monitor and Detector cards. This standardises the boards maintaining consistency in their designs, and so minimising errors.

C. The Detector Card

This card (See Fig. 3) is responsible for capturing the neutron position events and histogramming them. In effect, it

reproduces the functionality of the DAE-I Instrument and System Crates onto a single card. As detector systems expand, it would then be a matter of duplicating extra cards of this type in the Control Crate. The functionality follows almost exactly as for the DAE-I system. Where the difference lies is in the use of FPGA's which allow DAE-I board functionality to be implemented almost as a single chip.

For the generation of the time channels a 64K*32Bit SRAM lookup table is used under the control of the TCG FPGA. This increases the number of time channels available to 64K Time Channels per Acquisition Frame. Integrating much of the TCG scalar and control logic onto a single chip allows a minimum time channel resolution of 100nS to be achieved. Widening the width of the lookup table from 20Bits (DAE-I) to 32Bits means a maximum acquisition frame length of 128 Seconds is possible.

The DIM module functionality in DAE-I can similarly be achieved in an FPGA solution. A personality PROM configures the FPGA allowing it to function either as a DIM1 or DIM2. Upto to sixteen Detector Input Gate Arrays (DIGA's) can be fitted on the card each handling 4096 detectors in the DIM2 format. Each DIGA will have a 32Bit data capture latch (16Bit for time channel, 16Bit for position) and a 32Deep*32Bit true FIFO. This FIFO will enable the 20MHz peak event rate to be maintained whilst using slower CMOS technology as a oppose to the ECL technology used to achieve this on DAE-I.

Arbitration of the DIGA's to allow their events to be written into the PPFMs will be controlled by the Arbiter FPGA. The DAE-I arbitration method is priority based but this has led to some problems with the EVS glass scintillator detector event rates. For DAE-II a round-robin method of arbitration will be employed. Also included in this Arbiter will be a Detector Raw/Good Neutron Counters with registers to allow start and stop times between which event data is collected. This register will be a useful diagnostic aid to see that the card is collecting data. Access to these counters would be simpler in operation than obtaining the same information from the histogram.

The final FPGA in this area of DAE-II is a veto counter FPGA that will log the DIGA FIFO Overflow vetoes. This will allow the identification of a noisy detector to be more accurately pinpointed.

The DAE-II PPFM's will have their size increased from 20K to 64K allowing many more events to be collected in a frame. The FPGA functionality is expanded to allow a user-settable maximum number of events per frame to be collected (PPFM overflow veto). This is to trap a noisy detector from corrupting a frame and hence the spectra (especially when detectors are ganged). It may not be possible to predict the actual number of events per frame that will occur, hence the incorporation into this FPGA of a counter that simply logs the maximum number of counts occurring in a frame. This counter could log the maximum value readout

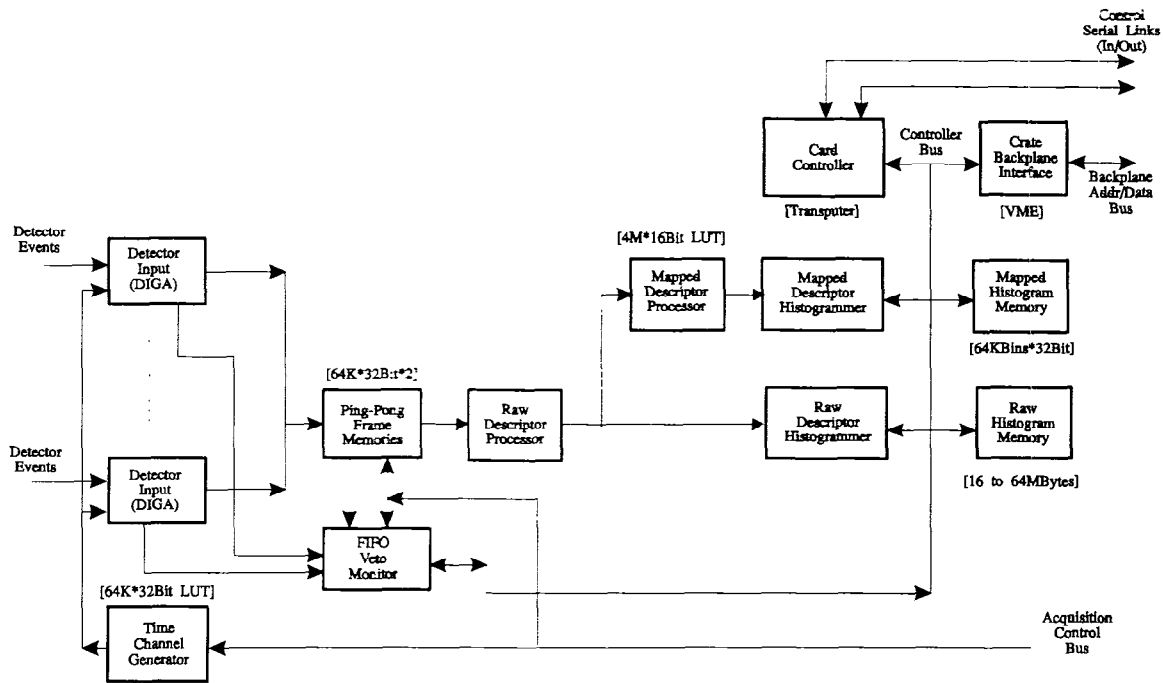


Fig. 3. Detector Card Block Diagram

over the first hour of the run, a tolerance value then added to that value and the result being used to set-up the PPFM overflow veto.

Within the Raw Descriptor Processor is a 2KDeep*32Bit FIFO used to buffer the block moving of descriptors from the PPFM through the Descriptor Processor to the Histogrammer. The pipeline architecture of the Descriptor Processor, Histogrammer and the actual histogramming process to the Histogram memory tends to slow the transfer of descriptors. Hence the need for the FIFO to maintain a balanced throughput. The Descriptor Processor also contains a coarse detector position mapping table. This is needed to map the detectors efficiently to the histogram memory. The mapping calculation is performed by a multiplier/accumulator device which can be set-up to perform either the $(T_{max} * P) + T$ or the $(P_{max} * T) + P$ algorithm.

After coming out of the Descriptor Generator the raw histogram descriptors are passed into another FIFO before going into the Raw Histogram Histogrammer. This FIFO's purpose is to ensure there is no holding up of data transfer, when the Transputer is accessing the Histogram Memory. This was a problem with DAE-I where data transfer from the PPFM was being held up when the FEM was doing large block reads of the histogram memory.

A Raw Histogrammer FPGA takes the Raw Histogram Descriptor and performs the Read-Increment-Write operation on the Histogram Memory. The size of the histogram memory will be either 4M*32Bit or 16M*32Bit depending on the instrument requirements, using the latest 16MBit DRAM's in an array. This means that 4M or

16MHistogram channels per detector card will be available to the user.

A design departure from the DAE-I architecture is the introduction of a Mapped Histogram Lookup table, Histogrammer and Histogram Memory. With higher density DRAM memory devices available, large lookup tables can be created in a small real estate area. What the Mapped Histogram Lookup table allows is the mapping of the Raw Histogram Descriptors to a particular bin. This means that focusing of time shifted detector spectra can be done to produce a single spectra achieving a significant reduction in data. The 64KBin Mapped Histogram memory can then be used to check instrument data integrity quickly rather than having to search the full Raw Descriptor Histogram which could be processor intensive.

The second departure from DAE-I is the use of an on-board processor to manipulate data in the Raw histogram. Transputers were chosen as the processor because of their ability to work in parallel. It is envisaged that many detector cards will be used with Transputers linked together via the backplane by their serial links. At a minimum level a single command could be passed to each, instructing the clearing the histogram memories. A second higher level use of the Transputer would be the data reduction of the raw histogram using Delta (shift level) encoding and/or Huffman encoding data compression techniques. On-board EPROM would contain a suite of programs that could be selected to perform the desired operation.

D. Monitor Card

This card almost follows exactly as for the Detector card, in that it carries the same VME/VXI interface with the option of a Transputer to be fitted to the board for future processing requirements.

The data acquisition parts are scaled down versions found on the Detector card. Four monitors will be accommodated each having the same PPFM, Descriptor Processor, Histogrammer structure as the Detector card. In splitting the monitors into four separate identical data acquisition circuits a gain in acquisition and data transfer speed is possible. It also allows redundancy should a monitor circuit fail. The Histogram memory for each monitor is 64KBins*32Bit in width and the same PPFM overflow veto setting and logging as found on the Detector card can be made.

V. SUMMARY

The need for the DAE-II second generation data acquisition electronics system is clear. The current DAE-I is unable to meet the future instrument detector and operational requirements. Implementing DAE-II in VXI with its electromagnetic interference suppression and the PCB method of manufacture will bring reliability benefits. The use of PLD and FPGA re-programmable technologies will allow the design to accommodate future changes. The project schedule is for the Instrument SANDALS to have an operational DAE-II system for the 3rd Quarter of 1994.

VI. REFERENCES

- [1] VMEBus International Trade Association, VXIBus System Specification, Rev 1.3, July 14, 1989
- [2] XILINX, The Programmable Gate Array Databook, 1992
- [3] Small Computer System Interface (SCSI-II), American National Standards, X3t(.2/86-109 Rev.10h, Nov 11, 1991
- [4] INMOS, The Transputer Databook, 2nd Edition 1989